

Docket No.: 2257-0260PUS1
(PATENT)

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:
Toshiyuki MAEDA et al.

Application No.: 10/582,936

Confirmation No.: 9823

Filed: June 15, 2006

Art Unit: 2838

For: CURRENT SUPPLY CIRCUIT, POLYPHASE
DRIVE CIRCUIT, METHOD OF DESIGNING
CURRENT SUPPLY CIRCUIT

Examiner: H. R. Behm

APPEAL BRIEF

MS Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

As required under § 41.37(a), this brief is filed more than two months after the Notice of Appeal filed in this case on May 7, 2009, or within one month from mailing of the Notice of Panel Decision from Pre-Appeal Brief Review in this case September 6, 2009, and is in furtherance of said Notice of Appeal.

The fees required under § 41.20(b)(2) are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains items under the following headings as required by 37 C.F.R. § 41.37 and M.P.E.P. § 1205.2:

- I. Real Party In Interest
- II. Related Appeals and Interferences
- III. Status of Claims
- IV. Status of Amendments

- V. Summary of Claimed Subject Matter
- VI. Grounds of Rejection to be Reviewed on Appeal
- VII. Argument
- VIII. Claims
- IX. Evidence
- X. Related Proceedings
- XI. Conclusion
- Appendix A Claims
- Appendix B Evidence
- Appendix C Related Proceedings

I. REAL PARTY IN INTEREST

The real party in interest for this appeal is:

DAIKIN INDUSTRIES, LTD.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in this appeal.

III. STATUS OF CLAIMS

A. Total Number of Claims in Application

There are 15 claims pending in application.

B. Current Status of Claims

1. Claims canceled: 0
2. Claims withdrawn from consideration but not canceled: 0
3. Claims pending: 1-15
4. Claims allowed: 0
5. Claims rejected: 1-15

C. Claims On Appeal

The claims on appeal are claims 1-15

IV. STATUS OF AMENDMENTS

Applicant did not file an Amendment After Final Rejection.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The present invention is directed to techniques for supplying polyphase current, and specifically, to a method and apparatus for reducing losses in a current supply circuit including an inverter having an insulated gate bipolar transistor (IGBT) element. (Spec. p. 3, ll. 3-5)

Independent claim 1 defines a current supply circuit applied with an AC voltage of a predetermined effective value voltage to output a polyphase AC current to a polyphase load of a predetermined rated power. The current supply circuit includes, *inter alia*, a polyphase inverter circuit including a series connection of two switching elements for each phase, and outputting said AC current of each phase from a node of said series connection (Fig 8, Spec. p. 22, ll. 3-11), wherein said switching element is selected to have a second breakdown voltage, said second breakdown voltage being twice a first breakdown voltage required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit (Spec. p. 22, ll. 3-18, Figs. 8 and Fig. 6), and wherein said switching element is selected to produce almost the same turn-on losses in a rated current value of said polyphase inverter circuit, said rated current value being obtained by dividing said rated power of said polyphase load by a voltage value being twice said effective value voltage as said turn-on losses, as turn-on losses based on dynamic losses required in regard to said switching element and said switching frequency of said inverter. (Spec. p. 19, l. 5 to p.20, l. 21, p. 22, ll. 3-18, Figs. 6 and 8)

Independent claim 5 defines a method of designing a current supply circuit applied with an AC voltage of a predetermined effective value voltage to output a polyphase AC current to a polyphase load of a predetermined rated power, said current supply circuit comprising a

polyphase inverter circuit, said polyphase inverter circuit including series connection of two switching elements for each phase, and outputting said AC current of each phase from a node of said series connection. (Spec. p. 22, ll. 3-18, Figs. 6 and 8) The method includes, *inter alia*, the steps of: (a) setting a current value as a rated current value of said polyphase inverter circuit, said current value being obtained by dividing said rated power of said polyphase load by a voltage value being twice said effective value voltage; (Spec. p. 19, l. 5 to p. 20, l. 21, Fig. 6) and (b) selecting said switching element having a second breakdown voltage based on said rated current value, said second breakdown voltage being twice a first breakdown voltage required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit. (Spec. p. 19, l. 5 to p. 20, l. 21, Fig. 6)

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

A. Claims 1-10 and 13-15 are rejected under 35 U.S.C. § 103(a) as being unpatentable over U. S. Patent No. 6,550,290 to Shimakage (“Shimakage”) in view of Japanese Publication No. JP 04-359890 to Makino (“Makino”) and Mitsubishi Application Note “Using Intelligent Power Modules” (“Mitsubishi Note 1”), further in view of Toshiba Application Guideline 15 (“Toshiba”).

B. Claims 11 and 12 are rejected under 35 U.S.C. § 103(a) as being unpatentable over Shimakage in view of Makino, Mitsubishi Note 1, and Toshiba, further in view of Mitsubishi Application Note “General Considerations for IGBT and Intelligent Power Modules” (“Mitsubishi Note 2”).

VII. ARGUMENTS

A. Claims 1-10 and 13-15 are patentable over the combination of Shimakage, Makino, Mitsubishi Note 1, and Toshiba because the Examiner fails to establish a *prima facie* case of obviousness.

In order to support a rejection under 35 U.S.C. § 103, the Examiner must establish a *prima facie* case of obviousness. To establish a *prima facie* case of obviousness three criteria must be met. First there must be some rationale to combine the cited references. Second, there must be a reasonable expectation of success. Finally, the combination must teach each and every claimed element. In the present case, claims 1-10 and 13-15 are not rendered unpatentable by the combination of Shimakage, Yashiro, Mitsubishi Note 1 and Toshiba for at least the reason that the combination fails to disclose each and every claimed element as discussed below.

Independent claim 5

Independent claim 5 defines a method of designing a current supply circuit supplied with an AC voltage of a predetermined effective value voltage. The method includes, *inter alia*, selecting switching elements having a breakdown voltage based on a rated current value, the breakdown voltage being *twice* the *breakdown voltage required* of the switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit.

Nowhere in any of the cited references is there any disclosure or suggestion of using a switching element with a breakdown voltage that is *twice* the *breakdown voltage required* when a DC voltage is input to said polyphase inverter circuit as claimed (i.e., a second breakdown voltage is twice a first breakdown voltage).

In response to Applicant's arguments, the Examiner asserts that Toshiba "teaches using a 1700V rated IGBT for a required voltage of 600Vac nominal." Furthermore, the Examiner asserts that "[s]ince the required voltage of 600Vac is rectified to 848V, the breakdown voltage

is taught to be twice the voltage required.” The Examiner’s assertion is unfounded for the following reason.

Although Toshiba discloses using a 1700V rated IGBT for an input voltage of 600V as suggested by the Examiner, which *arguendo*, results in a breakdown voltage twice that of the *input* voltage, the claimed invention requires that the breakdown voltage be twice that of the *required breakdown* voltage, not the *input* voltage. Conventionally, in the 600V drive of the Toshiba, the required breakdown voltage would be 1200V. However, as noted by Toshiba due to various factors the required breakdown voltage could easily exceed 1200V resulting in the need for the 1700V IGBTs. Therefore, in order for Toshiba to disclose using a breakdown voltage twice the *required breakdown* voltage, Toshiba would have to disclose using a 2400V IGBT instead of the required 1200V, not a 1700V IGBT. The fact that Toshiba *arguendo* discloses a breakdown voltage twice the *input* voltage is not equivalent to teaching a breakdown voltage twice the *required breakdown voltage* as claimed. It is clear from the Examiner’s arguments that he has incorrectly interpreted that claims as requiring the breakdown voltage be twice the *input* voltage instead of twice the *required breakdown voltage* as clearly recited in claim 5.

Since none of the cited prior art teaches or suggests “selecting said switching element having a second breakdown voltage based on said rated current value, said second breakdown voltage being twice a first breakdown voltage required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit” as claimed, the combination of these four reference cannot possibly disclose or suggest said feature. Therefore, even if one skilled in the art has some rationale to combine Shimakage, Yasuhiro, Mitsubishi Note 1 and Toshiba, the combination would still fail

to render claim 5 unpatentable because the combination fails to disclose or suggest selecting switching elements having a breakdown voltage *twice the required breakdown voltage* as claimed.

Claims 1-4, 6-10 and 13-15

Independent claim 1 and claims 2-4, which depend variously there from, define a current supply circuit that includes, *inter alia*, a switching element having a second breakdown voltage, said second breakdown voltage being twice a first breakdown voltage required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit. Accordingly, claims 1-4 are patentable over the combination of Shimakage, Yasuhiro, Mitsubishi Note 1 and Toshiba for the same reasons presented above with respect to claim 5.

Claims 6-10 and 13-15 variously depend from independent claim 5. Therefore, claims 6-10 and 13-15 are patentable over the combination of Shimakage, Yasuhiro, Mitsubishi Note 1 and Toshiba for the same reasons presented above with respect to claim 5.

B. Claims 11 and 12 are patentable over the combination of Shimakage, Makino, Mitsubishi Note 1, Toshiba, and Mitsubishi Note 2 because the Examiner fails to establish a *prima facie* case of obviousness.

Claims 11 and 12 variously depend from independent claim 5. Therefore, claims 11 and 12 are patentable over the combination of Shimakage, Yasuhiro, Mitsubishi Note 1 and Toshiba for at least those reasons presented above with respect to claim 5. Although Mitsubishi Note 2 may disclose how to determine the switching loss in an IGBT circuit, Mitsubishi Note 2 fails to overcome the deficiencies of Shimakage, Yasuhiro, Mitsubishi Note 1 and Toshiba.

Since none of the cited prior art teaches or suggests “selecting said switching element having a second breakdown voltage based on said rated current value, said second breakdown voltage being twice a first breakdown voltage required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit” as claimed, the combination of these five reference cannot possibly disclose or suggest said feature. Therefore, even if one skilled in the art has some rationale to combine Shimakage, Yasuhiro, Mitsubishi Note 1, Toshiba, and Mitsubishi Note 2, the combination would still fail to render claim 5 unpatentable because the combination fails to disclose or suggest selecting switching elements having a breakdown voltage *twice the required breakdown voltage* as claimed.

VIII. CLAIMS

A copy of the claims involved in the present appeal is attached hereto as Appendix A. As indicated above, the claims in Appendix A

IX. EVIDENCE

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

X. RELATED PROCEEDINGS

No related proceedings are referenced in II. above, or copies of decisions in related proceedings are not provided, hence no Appendix is included

XI. CONCLUSION

For at least those reasons presented above, Appellant respectfully requests reversal of the Examiner’s rejections of claims 1-15.

The Commissioner is hereby authorized to charge any appropriate fees under 37 C.F.R. §§ 1.16, 1.17, and 1.21 that may be required by this paper and to credit any overpayment to Deposit Account No. 02-2448.

Dated: September 4, 2009

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APPENDIX A

Claims Involved in the Appeal of Application Serial No. 10/582,936

1. A current supply circuit applied with an AC voltage of a predetermined effective value voltage to output a polyphase AC current to a polyphase load of a predetermined rated power, said current supply circuit comprising:

a polyphase inverter circuit including a series connection of two switching elements for each phase, and outputting said AC current of each phase from a node of said series connection, wherein

said switching element is selected to have a second breakdown voltage, said second breakdown voltage being twice a first breakdown voltage required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit, and

said switching element is selected to produce almost the same turn-on losses in a rated current value of said polyphase inverter circuit, said rated current value being obtained by dividing said rated power of said polyphase load by a voltage value being twice said effective value voltage as said turn-on losses, as turn-on losses based on dynamic losses required in regard to said switching element and said switching frequency of said inverter.

2. The current supply circuit according to claim 1, wherein said AC voltage of said predetermined effective value voltage is a single phase, and said current supply circuit further comprises a voltage doubler rectifying circuit performing voltage doubler rectification on said

AC voltage of said predetermined effective value voltage to output a rectified voltage to said polyphase inverter circuit.

3. The current supply circuit according to claim 2, wherein
said voltage doubler rectifying circuit and said polyphase inverter circuit are
modularized.

4. A polyphase drive circuit comprising:
the current supply circuit according to claim 3; and
a polyphase motor for 400 V supplied with current from said polyphase inverter circuit.

5. A method of designing a current supply circuit applied with an AC voltage of a predetermined effective value voltage to output a polyphase AC current to a polyphase load of a predetermined rated power, said current supply circuit comprising a polyphase inverter circuit, said polyphase inverter circuit including series connection of two switching elements for each phase, and outputting said AC current of each phase from a node of said series connection, and
said method comprising the steps of:

(a) setting a current value as a rated current value of said polyphase inverter circuit, said current value being obtained by dividing said rated power of said polyphase load by a voltage value being twice said effective value voltage; and

(b) selecting said switching element having a second breakdown voltage based on said rated current value, said second breakdown voltage being twice a first breakdown voltage

required of said switching element when a DC voltage obtained by performing full-wave rectification on said AC voltage is input to said polyphase inverter circuit.

6. The method of designing a current supply circuit according to claim 5, wherein said AC voltage of said predetermined effective value voltage is a single phase, and said current supply circuit further comprises a voltage doubler rectifying circuit performing voltage doubler rectification on said AC voltage of said predetermined effective value voltage to output a rectified voltage to said polyphase inverter circuit.

7. The method of designing a current supply circuit according to claim 5, wherein in said step (b), as a switching frequency (fsw) of said inverter increases, said switching element is selected in a range with low turn-on losses (Esw(on)) in said rated current value.

8. The method of designing a current supply circuit according to claim 7, wherein said step (b) further comprises the steps of:

(b-1) setting turn-on losses (Esw(on) = Esw / 2) based on dynamic losses (Psw) required in regard to said switching element and said switching frequency (fsw) of said inverter; and

(b-2) selecting said switching element having said second breakdown voltage, and producing almost the same turn-on losses as said turn-on losses in said rated current value set in said step (b-1).

9. The method of designing a current supply circuit according to claim 6, wherein in said step (b), as a switching frequency (fsw) of said inverter increases, said switching element is selected in a range with low turn-on losses (Esw(on)) in said rated current value.

10. The method of designing a current supply circuit according to claim 9, wherein said step (b) further comprises the steps of:

(b-1) setting turn-on losses (Esw(on) = Esw / 2) based on dynamic losses (Psw) required in regard to said switching element and said switching frequency (fsw) of said inverter; and

(b-2) selecting said switching element that has said second breakdown voltage, and produces almost the same turn-on losses as said turn-on losses in said rated current value set in said step (b-1).

11. The method of designing a current supply circuit according to claim 5, wherein said switching element is an IGBT element, and in said step (b),

an increment (ΔEsw) of turn-on losses in rated current value of said IGBT element having said second breakdown voltage with reference to turn-on losses (EL) in rated current value of said IGBT element having said first breakdown voltage is defined as a divisor,

the product of a first value, a second value, and a third value is defined as a dividend, said first value ($VL - \Delta Vce$) being obtained by subtracting an increment (ΔVce) of a saturation voltage of said IGBT element having said second breakdown voltage with reference to a saturation voltage (VL) of said IGBT element having said first breakdown voltage from said saturation

voltage (VL), said second value (Icp) being a maximum value of an output current of said inverter in terms of sinusoidal wave, and said third value being ($\pi/16$), and

 said IGBT element having said second breakdown voltage is selected in an area with a lower switching frequency (fsw) of said inverter than the result obtained by dividing said dividend by said divisor.

12. The method of designing a current supply circuit according to 6, wherein
 said switching element is an IGBT element, and in said step (b),
 an increment (ΔE_{sw}), multiplied by a factor of ($2 / \pi$), of turn-on losses in rated current value of said IGBT element having said second breakdown voltage with reference to turn-on losses (EL) in rated current value of said IGBT element having said first breakdown voltage is defined as a divisor,

 a value is defined as a dividend, said value ($P_d + (VL - \Delta V_{ce}) \cdot I_{cp} / 8$) being obtained by adding losses (P_d) for one diode included in said voltage doubler rectifying circuit (22) to the product of a first value, a second value, and a third value, said first value ($VL - \Delta V_{ce}$) being obtained by subtracting an increment (ΔV_{ce}) of a saturation voltage of said IGBT element having said second breakdown voltage with reference to a saturation voltage (VL) of said IGBT element having said first breakdown voltage from said saturation voltage, said second value (Icp) being a maximum value of an output current of said inverter in terms of sinusoidal wave, and said third value being ($1 / 8$), and

said IGBT element having said second breakdown voltage is selected in an area with a lower switching frequency (fsw) of said inverter than the result obtained by dividing said dividend by said divisor.

13. The method of designing a current supply circuit according to claim 11, wherein said inverter has said switching frequency (fsw) set to 7 kHz or less.

14. The method of designing a current supply circuit according to claim 5, wherein said predetermined effective value voltage is 200 V, and said first breakdown voltage is 600 V.

15. The method of designing a current supply circuit according to any one of claims 5 to 14, wherein said switching element is an IGBT element.

APPENDIX B

No evidence pursuant to §§ 1.130, 1.131, or 1.132 or entered by or relied upon by the examiner is being submitted.

APPENDIX C

No related proceedings are referenced in II. above, hence copies of decisions in related proceedings are not provided.